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THESIS OF BACHELOR

论文题目：通用薄膜晶体管紧凑模型的研究

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通用薄膜晶体管紧凑模型的研究

摘要

基于新材料（包括金属氧化物半导体、有机半导体等）的薄膜晶体管（thin-film transistor, TFT）技术成为基础研究与产业应用关注的热点。这些新型 TFT 技术的发展一方面有望满足未来显示技术多元化发展的要求，另一方面基于玻璃、塑料等基底的大面积电子集成，能够带动一系列以发展更友好“人—机—环境”界面为目标的新兴信息电子技术的研究和产业发展方向，如：柔性电子、印刷电子、可穿戴电子等等。面向 TFT 技术在电路与系统中的应用，需要发展 TFT 的紧凑器件模型，以能够集成到商业化电路仿真工具中，用于预测和优化所设计 TFT 电路的性能。目前，已有大量的研究针对不同材料和工艺技术的 TFT 器件发展其相应的紧凑模型。然而，这些针对性强的模型难以适用于不同材料或工艺的 TFT 技术，而且包含的模型参数较多，提取的过程比较复杂，对所给 TFT 器件难以有效率地完成模型参数的准确提取。此外，由于这些针对不同 TFT 技术的模型所定义的模型参数的不同，所以无法直观地用于表征和比较不同 TFT 之间的性能。

针对这些问题，本论文建立了一个通用的 TFT 模型，适用于不同材料体系和工艺技术的 TFT 器件。该模型直接加入了亚阈值摆幅的表达式，从而比传统 TFT 模型能够更合理的模拟 TFT 在亚阈值区域的特性，而且所需要的模型参数少，参数提取过程简单。为了验证其准确性，该模型被应用于几种不同的 TFT 器件技术，包括有机小分子半导体 TFT、聚合物半导体 TFT 以及铟镓锌氧（IGZO）非晶氧化物半导体 TFT。模型均能够很好的与实验结果拟合，证明了该模型的通用性。最后通过 Verilog-AMS 语言将该模型嵌入到商业化的电路仿真工具 HSPICE 中，并作为验证 应用于一个 IGZO TFT 电路的设计，仿真结果与实验测试结果能够很好的吻合。

关键词：薄膜晶体管，通用模型，Verilog-AMS，SPICE，电路仿真

A UNIVERSAL COMPACT MODEL FOR THIN-FILM TRANSISTOR

ABSTRACT

Thin-film transistor (TFT) technologies based on various new materials, including organic and metal oxide semiconductors, have attracted great attention from both industry and academia. Development of these new TFT technologies can help to meet the demands of realizing advanced flat panel displays of different new features, as well as create many novel electronics applications towards friendly "human-machine-environment" interfaces based on the large area electronics integration on glass, plastic and other arbitrary substrates. To develop TFT circuits and systems for these potential applications, accurate compact TFT models are required to be integrated into the commercial circuit simulator to simulate and predict the performance of the designed circuits. Currently, there have already been lots of work on developing compact models specifically for different TFT technologies. However, very few of these specific models can be easily adopted to a wide range of TFT technologies. With many physical parameters in these models, a relatively complex parameter extraction procedure is also required, which makes it difficult to efficiently obtain the model parameters for a given TFT technology. Moreover, since the models for different TFT technologies define different model parameters, they are not able to be used for intuitively characterizing and comparing the performance of different technologies.

To address these issues, this thesis develops a universal TFT model applicable to a wide range of TFT technologies. The model includes a substhreshold swing expression, and can simulate the device behavior in the subthreshold region more reasonably. The model uses much fewer model parameters, and thus a simple parameter extraction procedure. To prove its accuracy, the model is applied to various TFT technologies, including small molecule organic TFTs, polymer TFTs and amorphous indium gallium zinc oxide (IGZO) TFTs. In all cases, the model

can fit the experimental results very well, indicating its universality. Finally, the model is implemented into the commercial circuit simulator HSPICE using Verilog-AMS, and used for simulating an IGZO TFT circuit. The simulation results agree well with the measurements.

Key words: Thin-film transistor, compact model, Verilog-AMS, SPICE, circuit simulation

Contents

Chapter One Introduction

This chapter firstly provides an overview of thin-film transistors (TFTs) including the applications, several key TFT technologies, and different device structures for TFTs, then describes the important of developing compact models for TFTs and the motivation of this thesis. Finally, the organization of this thesis is introduced.

1.1 Overview of TFT Technologies

After more than five decades of development, the TFT has already become an essential semiconductor technology, especially for its application in flat panel displays. In 2013, the total area of produced TFT-LCD display panels that manufacturers had made is about 141 million square meters, containing about 10^{16} TFTs [1]. This huge TFT display industry has already become one of the most important economy pillars in modern society, and is continuously growing.

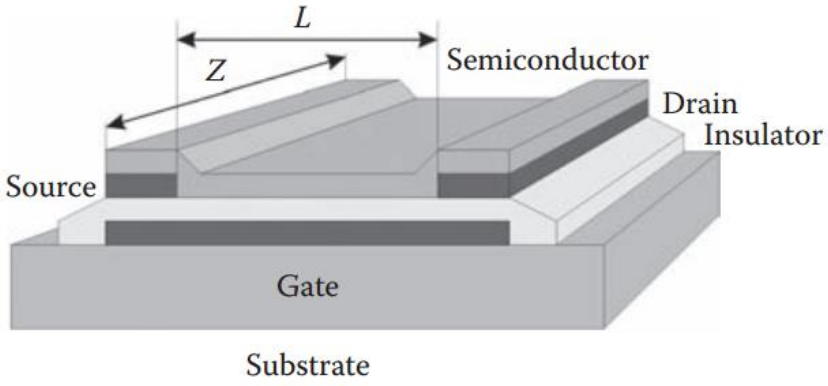

Fig 1 Basic Structure of TFT [2]

Like MOSFET, the TFT is composed of gate, source, drain, insulator and semiconductor. As shown in Fig.1, the active layer of this device is the semiconductor layer located between source and drain, this is the place where the conducting channel is formed. The length of source and drain is called the channel width *W*, and the vertical distance between source and drain is called the channel length *L*. An insulator layer is placed between gate and source (drain), which forms a metal insulator

semiconductor (MIS) structure.

Among the many structures designed for TFTs, the most popular three are the bottom gate bottom contact (BGBC), the bottom gate top contact structures (BGTC) and the top gate bottom contact (TGBC). The structures of all the devices used in this thesis is one of the three structures. Fig 2 shows the difference between a top-contact structure and a bottom-contact structure. Generally, the top contact structure can provide a larger current than bottom contact due to a comparative small contact resistance [3]. But the bottom contact structure is easier to be manufactured because its semiconductor layer is deposited at the last step. And this layer will not be exposed to other chemicals that been used in the fabrication of other lower layers.

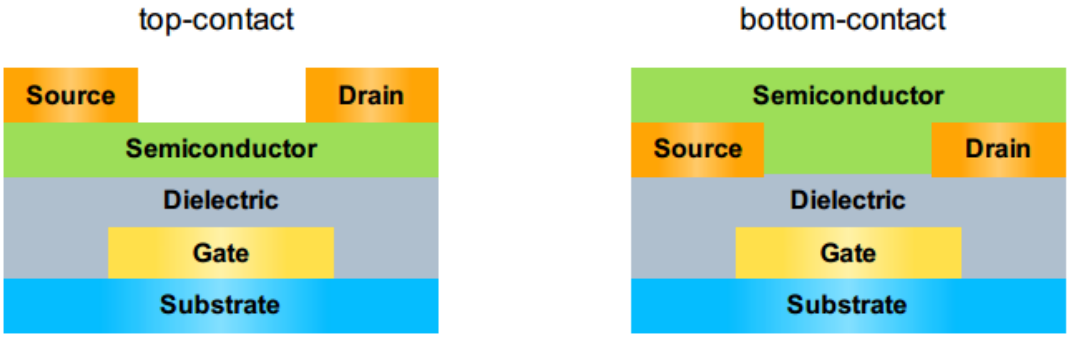

Fig 2 Illustrations of the bottom gate top contact and the bottom gate bottom contact structures [4]

There are a considerable number of materials that can be selected as the semiconductor layer of TFTs. As shown in Fig.3, each kind of those materials have their own characteristics. Ploy-Si TFT has high mobility but it needs high temperature processes. Organic Thin Film Transistor (OTFT), on the contrary, can be made in low temperature but its mobility is relative low. Some Oxide TFTs have extremely high transparency, which enables them to fabricate the transparent display. a-Si TFT is famous for good uniformity and it has already been used in display panel mass production. Besides that, a great deal of new material are being used to fabricate TFTs, like graphene, MoS_2 and some newly-synthetized organic material. With lots of efforts poured into this area, mobility has increased swiftly and process temperature has been cut at a fast pace in the past few decades.

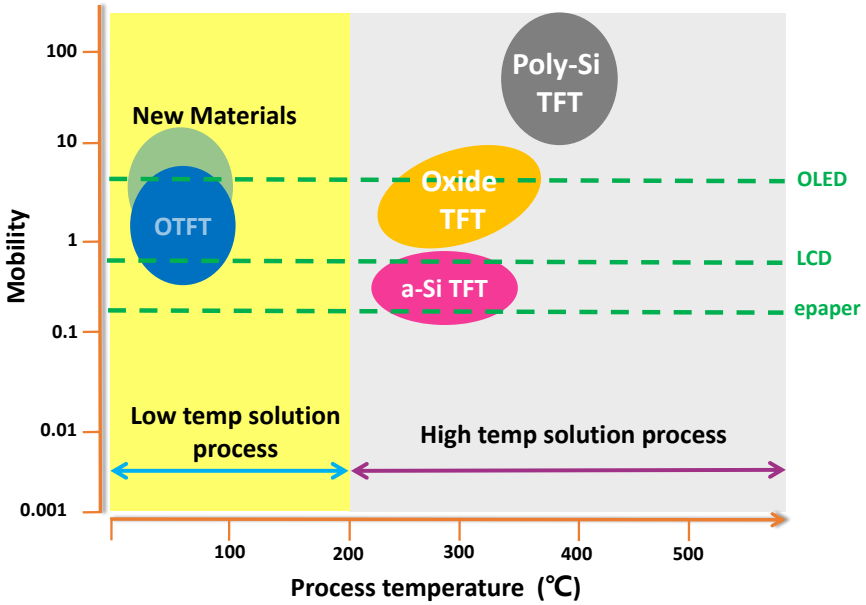

Fig 3 Mobility, process temperature and potential application of typical TFT materials [5]

1.1 Compact Models for TFTs

The diversity of TFTs allows us to choose suitable types of TFTs according to different application situations. Although diversity of TFT bring us with conveniences, it caused troubles in other aspects, the modeling of TFTs is a good example.

Many models have already been developed for some TFTs which have mature processes [6] ~ [8]. Those existing TFT models is becoming more sophisticated at the cost of a growing number of required parameters. Besides that, parameters extraction is more complex than before. This complication is partially caused by the existence of unique physical phenomena in different semiconductor materials. As a result, those sophisticated models cannot be applied to other material, and different parameters extraction methods of those models make evaluation between different kinds of TFT untrustworthy. More importantly, newly developed devices like all solution-processed OTFT does not have a specific model, and it will not have one in a short time. The lack of model severely lagged the implementation of new devices in circuit.

Regardless of the difficulties in establishing individualized model for different kinds of TFT, substantial progress has been made to understand and model the unique

physical phenomena in different TFT semiconductors. Academically, working principles of new TFTs like OTFT and indium gallium zinc oxide (IGZO) TFTs have been carefully investigated, and some channel conducting theories have already been proposed [9] ~ [10]. However, even with those theories, we still do not have an accurate model for some of those new devices.

1.1 Motivation

To meet the requirement of integrating new TFTs into the commercial circuit simulator to simulate and predict the performance of the designed circuit, a compact model is required. Since we cannot fully understand the physical working mechanism of new TFTs, a universal compact model which can reflect the essence of different TFTs will be of great importance to the new TFTs.

Therefore, the universal TFT model is required to possess the following features:

1) Accurate, can characterize the behavior of TFTs.
2) Simple, with as few parameters as possible. But parameters should having certain physical meaning, and they should be instructive to circuit design. No comprise should be made with essence in overall TFT behavior, but some freedom should can be given for simplification.
3) Analytical, without differentials or integrals.
4) Easy for parameter extraction.
5) Universal for various TFT technologies.
6) Upgradeable and reducible.

1.1 Organization of This Thesis

This dissertation consists of five chapters. This first chapter makes an introduction on TFT, this introduction covers its working principle, device structures, unique advantages and potential applications. The goal of this research is also stated in this chapter. Chapter two is the core of this dissertation, it details the establishment of mathematical model. Equation derivation process and the smoothing function forms the major part of this chapter. Chapter three introduce how we implement this

model into the circuit simulator (HSPICE). Chapter four describes the parameter extraction method of this model. A MATLAB-HSPICE platform has been developed for the convenience of parameters extraction. The order of parameter extraction is enclosed too. Chapter five verified this model with different kinds of TFTs, including small molecule OTFT, polymer OTFT and IGZO TFT. Circuit built with this model is tested based on HSPICE in Chapter six. In the last chapter, it concludes the contribution and limitation of the research, the direction and expectations of the future pursuit is also briefly discussed.

Chapter Two Establishment of Mathematical Models

Simplicity and accuracy are two conflicting objectives of TFT modeling. To obtain a good TFT model, appropriate tradeoffs are of great importance. Since the purpose of this work is to establish a universal TFT model, it will not be necessary for us to describe all the unique physical phenomena of different semiconductor materials in this model. Instead, several fitting parameters will be added into its parameters list, those parameters can change the appearance of the curve, and they are used to represent the minor physical mechanisms that may lead to the varying in the shape of the curve. With those parameters, plenty of model physical parameters can be reduced. Based on this idea, the mathematical model is derived, by applying some simplification, the final form of the current equations are acquired.

2.1 Derivation of current-voltage equations

This part is to derive the current-voltage equations of the TFTs in different operation regions: ON-state region (including saturation region and linear region), subthreshold region and OFF-state region. The used mobility model is firstly introduced.

2.1.1 Mobility Model

In the conducting channel of TFT, charge transport mechanism is limited by the localized states induced by defects and impurities in the semiconductor. And there are already numbers of theories to explain this charge transport mechanism and summarized it in a mathematical form, among them, there are two most widely accepted theories: multiple trapping and thermal release (MTR) [11] and variable range hopping (VRH) [12], which are for semiconductor materials with different levels of localized states. Based on both models, the mobility can be given in a universal form as equation (1).

$$\mu_{eff} = \mu_0 (\frac{V_G - V_T}{V_{aa}})^{\gamma} \quad (1)$$

Here, V_G is the voltage applied on the gate electrode, μ_0 is low field mobility, γ is the mobility enhancement parameter and V_{aa} is used as a reference parameter.

2.1.1 Linear Region Model

After relationship between gate voltage and channel conductivity is built with a mobility model, further analysis on the impact of source-drain voltage on channel current can be carried out. Considering the device only vary along the direction of channel, based on Gauss's law and charge conservation, the charge density Q(x) induced by gate voltage can be given by:

$$Q(\mathrm{x}) = C_{OX}(V_G - V_T - V(\mathrm{x})) \quad (2)$$

Where x is the coordinated along the channel, C_{OX} is the gate capacitance per unit area and V(x) is the potential in the semiconductor layer of the TFT. The function for mobility can be simplified to equation 3:

$$\mu_{eff} = \mu_r (V_G - V_T)^{\gamma} \quad (3)$$

μ_r is a reference whose unit is cm^2/V^3 s, and its expression is μ_0 / V_{aa}^{γ}. This mobility equation is of significant importance for compact modeling and it will be used in this dissertation. Applying the well-established concept for charge drift, the current per unit width in the TFT can are given in equation 4:

$$\frac{I_D}{W} = \mu_{eff} Q(\mathrm{x}) |E(\mathrm{x})| \quad (4)$$

where W is the channel width of TFT. At the position x in the channel, 0 < x < L, E(x) is the magnitude of electric field in the organic semiconducting film. Q(x) is the area charge density, μ_{eff} is the effective mobility. Then use equation 2 and 3 to substitute those parameters in equation 4, equation 5 can be acquired:

$$\begin{aligned} \frac{I_D}{W} &= \mu_r (V_G - V_S - V_t)^{\gamma} \times C_{OX}(V_G - V_t - V(\mathrm{x})) \times \left| \frac{\partial V(\mathrm{x})}{\partial x} \right| \\ &= \mu_r C_{OX} (V_{GS} - V_t)^{\gamma} (V_G - V_t - V(\mathrm{x})) \left| \frac{\partial V(\mathrm{x})}{\partial x} \right| \end{aligned} \quad (5)$$

In this equation, an important tradeoff that differs this model from other models is

made. Usually, a precise model require another variable $V_C(x)$ to replace V_S in the equation 5, this is due to the potential in the channel is different from the potential at source. However, this parameter $V_C(x)$ greatly increases the complexity of the final derived equation. After a short evaluation, it is found that the impact of this parameter on the essence in overall TFT behavior is sufficiently small to be ignored. To attain a simple function, this parameter is excluded in out model, the value of $V_C(x)$ is set as V_S instead.

The current along the conducting channel is a constant. By applying an integration along the channel length coordinate x on equation 5 can give us:

$$\frac{1}{W}\int_0^L (I_D)dx = \mu_r C_{OX}\int_0^L (V_{GS}-V_t)^{\gamma}(V_G-V_t-V(x))\left|\frac{\partial V(x)}{\partial x}\right|dx$$
$$= \mu_r C_{OX}\int_{V_S}^{V_D} (V_{GS}-V_t)^{\gamma}(V_G-V_t-V(x))dV_x$$
$$I_D\frac{L}{W} = -\mu_r C_{OX}\frac{1}{2}(V_{GS}-V_t)^{\gamma}(V_G-V_t-V(x))^2\Big|_{V_x=V_S}^{V_D} \quad (6)$$

Here, V_S is the potential of channel at source electrode. V_D is the potential of channel at drain electrode. Then we can derive the equation of the linear region model:

$$I_D = \mu_r\frac{W}{L}C_{OX}\frac{(V_{GS}-V_t)^{\gamma}(V_G-V_t-V_S)^2-(V_{GS}-V_t)^{\gamma}(V_G-V_t-V_D)^2}{2}$$

$$= \frac{1}{2}\mu_r\frac{W}{L}C_{OX}(V_{GS}-V_t)^{\gamma}[(V_{GS}-V_t)^2-(V_{GS}-V_t-V_{DS})^2] \quad (7)$$
$$= \mu_r\frac{W}{L}C_{OX}(V_{GS}-V_t)^{\gamma}V_{DS}(V_{GS}-V_t-\frac{V_{DS}}{2})$$

2.1.1 Saturation Region Model

On the occasion of $V_{DS}>V_{GS}-V_t$, the source-drain current will not follow the parabolic relationship that had been derived in linear region. The current becomes independent of V_{DS} in this region, and this region is defined as the saturation region.

The main reason accounts for the invalidation of linear region equation is the Q(x) in saturation region no longer follows the behavior of equation 2. Since $V_{DS}>V_{GS}-V_t$, the charges accumulation layer will disappear at the channel location x_a ($x_a<L$). This location x_a moves towards source with the increase of V_{DS}. Consequently, some of the

conditions in calculation should be changed to reflect this trend in Q(x).

Based on the former analysis, the upper and lower limits of the integral calculation (equation 5) are changed from [0, L] to [0, x_a], then the equation 5 can be reformed into equation 8:

$$\begin{aligned}\frac{1}{W}\int_0^L (I_D)dx &= \frac{1}{W}\int_0^{x_a} (I_D)dx \\ &= \mu_r C_{OX}\int_0^{x_a} (V_{GS}-V_t)^{\gamma}(V_G-V_t-V(\mathrm{x}))\left|\frac{\partial V(\mathrm{x})}{\partial x}\right|dx \\ &= \mu_r C_{OX}\int_{V_S}^{V_G-V_T} (V_{GS}-V_t)^{\gamma}(V_G-V_t-V(\mathrm{x}))dV_x \\ &= \frac{1}{2}\mu_r C_{OX}(V_{GS}-V_t)^{\gamma+2}\end{aligned} \quad (8)$$

Then the equation for saturation region can be given by:

$$I_D = \frac{1}{2}\mu_r C_{OX}\frac{W}{L}(V_{GS}-V_t)^{\gamma+2} \quad (9)$$

2.1.1 Subthreshold Region Model

Generally, subthreshold region is taken as a parasitic leakage in a region that would ideally have no current in digital circuits. In analog circuits, on the other hand, subthreshold region is an efficient operating region, and subthreshold is a valuable transistor working mode around which circuit functions are designed. [13]

To characterize the gate terminal controlled drain current behavior in subthreshold region, the concept of subthreshold slope is proposed. The plot of logarithmic channel current versus applied gate voltage under the condition of fixed drain-source voltage will exhibit approximately linear behavior in the subthreshold region. The slope of this curve is defined as the subthreshold slope. The reciprocal value of subthreshold slope is defined as the subthreshold swing (SS).

The widely-accepted subthreshold current of field effect transistor is proved and it follows the behavior of equation 10:

$$I_{Sub} = I_{S0}\frac{W}{L}\exp^{\frac{eV_{GS}}{kT}} \quad (10)$$

Here, I_{S0} is a reference current, it is usually the current at the beginning of

subthreshold region. *e* is the elementary charge and *KT* is the thermal energy. According to the definition of subthreshold swing, we can calculate it based on equation 10:

$$SS = \left(\frac{d \log(I_{Sub})}{dV_{GS}} \right)^{-1} = \frac{\ln 10 \left(I_{S0} \frac{W}{L} \exp^{\frac{eV_{GS}}{kT}} \right)}{I_{S0} \frac{W}{L} \exp^{\frac{eV_{GS}}{kT}} \frac{e}{kT}} = \frac{\ln 10 \cdot kT}{e} \quad (11)$$

It is very obvious that the subthreshold swing is a fixed value in equation 11. This is due to the influence of deep states density is ignored the in the derivation. Deep states are usually induce by the trap states between the surface of semiconductor and insulator. The influence of deep states in some TFTs is too big to be ignored and the value of deep states varies with different process and materials. From this point of view, being able to reflecting the influence of trap states' influence is an important requirement for this model. Hence, after taking the deep states density into consideration, we can obtain an empirical formula by adding the deep states parameter C_d:

$$SS' = \frac{\ln 10 \cdot kT}{e} (1 + \frac{C_d}{C_{OX}}) \quad (12)$$

Based on equation, the subthreshold drain current function can be modified so that the influence of deep states density could be reflected straightforwardly:

$$I_{Sub}' = I_{S0} \frac{W}{L} \exp^{\frac{eV_{GS}}{kT(1+\frac{C_d}{C_{OX}})}} \quad (13)$$

2.1.1 OFF Region Model

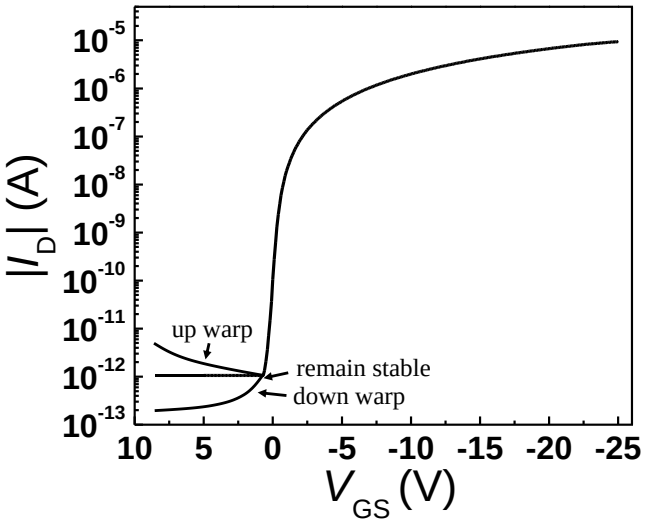

Fig 4 Three conditions of OFF state

For modeling, the drain current behavior at OFF region is no less important than other regions. However, up till now, there is no good physical explanation for the leakage current in the OFF state. Therefore, we set up an analytical model based on purely mathematics.

As shown in Fig.4, OFF region drain current behavior of devices that we have fabricated can be classified into three categories: up warp, down warp and remain stable. All those three conditions should be put into one equation to model the OFF state. A equation that have a similar appearance with subthreshold region equation is been used, the gate voltage dependent feature is also added into this equation

$$I_D = type \cdot (I_0 \cdot \frac{V_{DS}}{V_{DS0}}^{off_{23}}) \cdot 10^{off_{23} \cdot (-type) \cdot \mathrm{off}_{UP/DOWN} \cdot (-type \cdot (V_{GS} - V_{ON}))^{off_{11}}} \quad (14)$$

Here, type define n-type or p-type transistor, off_{23} reflects the control ability of gate voltage on drain current, $off_{\mathrm{UP/DOWN}}$ is the parameter to determine whether the subthreshold region current is up warp, down warp or remain stable. off_{11} determine how fast the current warps.

2.1 Channel Length Modulation

In the analysis we carried out in section 2.1.3, it is noticed that when the source-drain voltage increases in the saturation region, the length of accumulation layer of charges decreases. Which means the channel length parameter L is actually

controlled by V_{DS}. Assume that $L' = L - \Delta L$, and ΔL is proportionate to V_{DS}. Then equation 9 is modified to equation 15:

$$I_D = \frac{1}{2}\mu_r C_{OX}\frac{W}{L}(V_{GS}-V_t)^{\gamma+2}(1+\lambda V_{DS}) \qquad (15)$$

Here, λ is the channel length modulation parameter, it reflect the non-ideality of output characteristic in saturation region. In order to maintain the continuity between saturation regime and linear regime, this channel length modulation parameters should be added into the linear region too, the modified linear region equation is given by:

$$I_D = \mu_r \frac{W}{L} C_{OX}(V_{GS}-V_t)^{\gamma} V_{DS}(V_{GS}-V_t-\frac{V_{DS}}{2})(1+\lambda V_{DS}) \qquad (16)$$

2.1 Smoothing Function

In the procedures of building a compact model, selecting the right equation for different regions is just the first step. Simply putting this equations together will not be able to reflect TFT's true behavior, besides, the discontinuity between those regions will directly cause the error in the circuit simulator.

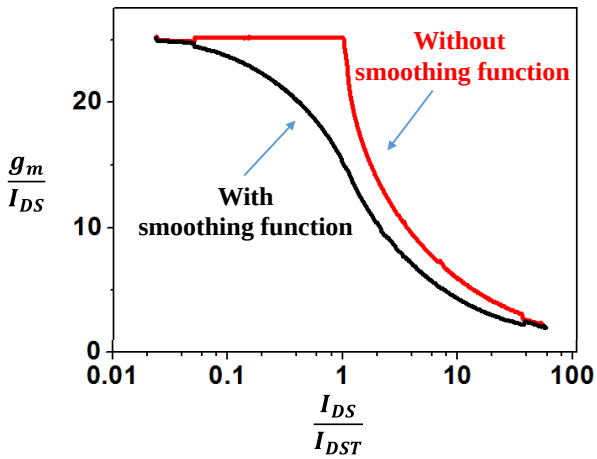

Fig 5 Influence of smoothing function on unity transconductance

Fig.5 shows the influence of smoothing function on the unity transconductance. Without a smoothing function, the transconductance suffers severely from the discontinuity. There is a sudden chance in the transistion region between saturation region and subthreshold region. The discontinuity will have a great chance to cause

the simulator a convergence error. Even if the simulator manages to generate a simulation result, as long as there is one single TFT in the system bias in a working region near this catastrophe point, the simulation result of whole system will not be able to reflect the true behavior of circuit.

Therefore, to ensure the first-order derivative of this model is continue, a smoothing function is highly desired. Among most commonly used smoothing functions, there are two kinds of widely accepted smoothing function which is parabolic smoothing function used in BSIM model and exponent smoothing function used in EKV model. Both of the smoothing function can assure the continuity of the transition region.

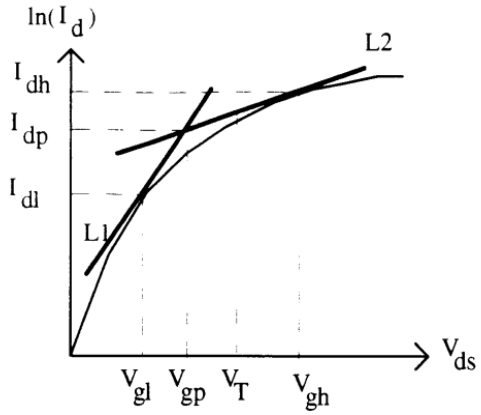

Fig 6 Illustration of parabolic smoothing function [14]

The basic idea of parabolic smoothing function is shown in Fig.6, this method is using a parabolic equation to fit the transition region between two different equations. In a model, the parameters of this parabolic function is composes of those parameters appears in the equations this smoothing function connects. As a result, finding out the parameters of this parabolic smoothing can be extremely difficult since other two equations are usually very complex in a TFT model. By using the MATLAB to solve this problem, parameters of this function are obtained. But the equations of those parameters are too complex to be used in the model, a complex equation also disobeys our purpose to build a relative simple model. Hence, we decide to renounce parabolic smoothing function.

The main reason we choose the EKV model smoothing function is it does not add

any new parameters and this smoothing function merges two function into one. The smoothing function of EKV model is shown in Equation 17:

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{GSTt}^{2}[\ln(1+e^{v})]^{2} \quad (17)$$

Here, $v = V_{GST}/V_{GSTt}$, and V_{GST}, V_{GSTt} are shown in the following equation:

$$V_{GST} = (V_{GS}-V_t)^{1+\frac{\gamma}{2}}\sqrt{1+\lambda V_{DS}}$$
$$V_{GSTt} = (V_{GS}-V_t)_t = \frac{2nkT(1+\frac{C_d}{C_{OX}})}{q} \quad (18)$$

Using this equation, subthreshold region and saturation region can be connected without any new fitting parameters.

When $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$, v will be large enough to make $ln(1+e^{v}) \approx v$, then equation 17 is approximately equal to the equation of saturation region, this procedure is stated in equation 19:

$$\begin{aligned} I_{DS} &= \frac{1}{2n}\mu C_{OX}\frac{W}{L}V_{GSTt}^{2}[\ln(1+e^{v})]^{2} \quad (v \text{ is large}) \\ &\approx K'\frac{W}{L}V_{GSTt}^{2}e^{2v} = K'\frac{W}{L}(V_{GS}-V_t)^{2+\gamma}(1+\lambda V_{DS}) \end{aligned} \quad (19)$$

When $V_{GS} \leq V_t$, v is small enough to make $ln(1+e^{v}) \approx e^{v}$, then equation 17 is approximately equal to the equation of subthreshold region, which is stated in equation 20:

$$\begin{aligned} I_{DS} &= \frac{1}{2n}\mu C_{OX}\frac{W}{L}V_{GSTt}^{2}[\ln(1+e^{v})]^{2} \quad (v \text{ is small}) \\ &\approx K'\frac{W}{L}V_{GSTt}^{2}e^{2v} = K'\frac{W}{L}V_{GSTt}^{2}e^{\frac{q(V_{GS}-V_T)\sqrt{1+\lambda V_{DS}}}{nkT(1+\frac{C_d}{C_{OX}})}} \end{aligned} \quad (20)$$

Now that the subthreshold region and saturation region in combined together with the smoothing function, the first order derivative of the transfer characteristic and can be continuous.

Next step is to implement the smoothing function in the transition region between linear region and saturation region. An intermediary parameter v_l has been draw into the equation so that linear region and saturation region could share the same smoothing equation. Here, $v_l = V_{GST}/V_{GSTtl}$, the definition for V_{GSTtl} is shown in

following equation:

$$V_{GSTl} = \sqrt{(V_{GS} - V_t)^{\gamma}(V_{GS} - V_t - \frac{V_{DS}}{2})V_{DS}(1+\lambda V_{DS})} \quad (21)$$

When the $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$, the transistor enters the linear region. v_l is large enough, $ln(1+e^{v_l}) \approx v_l$, then equation 17 is approximately equal to the equation of linear region which is shown in equation 22:

$$\begin{aligned} I_{DS} &= \frac{1}{2n}\mu C_{OX}\frac{W}{L}V_{GSTt}{}^2[\ln(1+e^{v})]^2 \quad (v \text{ is large}) \\ &\approx K'\frac{W}{L}V_{GSTt}{}^2 e^{2v_l} \\ &= K'\frac{W}{L}V_{DS}(V_{GS} - V_t)^{\gamma}(V_{GS} - V_t - \frac{V_{DS}}{2})(1+\lambda V_{DS}) \end{aligned} \quad (22)$$

Now the linear region and saturation region in combined together with the smoothing function, the first order derivative of the output characteristic and can be continuous.

The last job needed to be carried out here is connect OFF region function with subthreshold function. A function which has a similar express with subthreshold region is used, it is shown in equation 23:

$$I_{OFF1} = type \cdot (I_0 \cdot \frac{V_{DS}}{V_{DS0}}^{off_{23}}) \cdot 10^{off_{10} \cdot (type \cdot (V_{GS} - V_{on}))^{off_{11}}} \quad (23)$$

Some of the parameters in equation 23 is shared with equation 14, a new parameter off_{10} is added to reflect the slope change of this function. Notice that this function cannot guarantee the continuity of first-order derivative in the transition between OFF region and saturation region.

Chapter Three Implementation in Circuit Simulator

The most important function of compact models is to provide a bypass for circuit designers to predict the performance of circuit before the circuit is actually fabricated. This function can be realized by implementing the mathematical model into a circuit simulator. After a comprehensive consideration, Verilog-AMS is selected to be the description language due to its accuracy and publicity. Any simulators that support Verilog-AMS will be able to use the universal TFT model we developed.

2.1 Selecting a Model

The proposed universal TFT model have several versions that can be used in different circumstances. Some parameters have been reduced and equations are simplified in low ranking version. Those versions are designed for the conditions when the designer do not possess all data that required for parameter extraction, or these parameters of the model is not important from the designers' perspective.

Version 2.1: OFF region current equation is simplified. (OFF region current is independent from V_{DS})

Version 2.2: Mobility is a constant.

Version 2.3: The complete version of universal TFT model.

Those version can be selected at Verilog-A module declaration part in the input net list of HSPICE.

3.1 Convergence

As one of the key objectives in designing a good model, convergence of this model will influence of output of simulator directly. From a device model perspective, the proposed model should has continuity in the device current and in its first and second derivatives. From the simulator perspective, properly handling the GMIN and

DCGMIN control options can enhance the convergence.

Sometimes, convergence error will occurs in the simulation, which is especially common in the simulation with model written in Verilog-AMS. Altering GMIN and DCGMIN is one solution, using VZERO and EXPERT options is another option to solve this problem.

The model equations for N-type and P-type TFT inside the Verilog-AMS file is almost the same. A parameter called 'type' is used to reverse the polarities of V_{DS}, V_{GS} and V_t. The direction of current flow is also decided by this parameter.

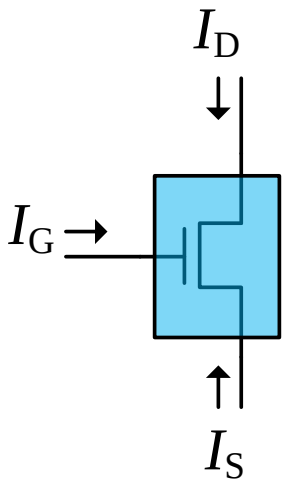

Fig 7 Illustration of TFT Current Convention

According to Fig.7, the current in the model are defined as follows:

- $I_D=I_{DS}-I_{GD}$;
- $I_G=I_{GS}+I_{GD}$;
- $I_S=-I_{DS}-I_{GS}$;

3.1 Equivalent Circuits

Commercialized transistor models are usually derived form a number of equivalent circuits, those circuits include DC, AC, transient and noise equivalent circuits. Though we do not have the ability to develop those models currently, the proposed model is still able to perform the transient and AC simulation at a lower accuracy.

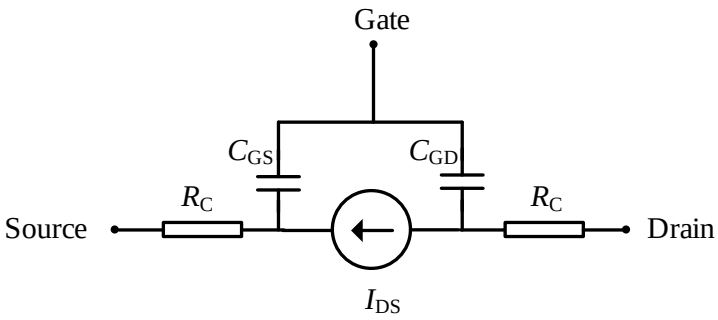

Fig 8 Equivalent circuit of the universal TFT model

The equivalent circuit of this model is shown in Fig.8, it consists of a voltage controlled current source, two contact resistances and two parasitic capacitor. The behavior of voltage controlled current source follows the equations we acquired before, its I-V characteristic is summarized in section 3.6.

3.1 Model Specification

The universal TFT model is written in Verilog-AMS and saved a '.va' file. To enable HSPICE call this model during simulation, this file is put under the same path with the '.sp' file. In the '.sp' file, a declaration of using the Verilog-AMS file should be stated first, and the model defined in the Verilog-AMS file need to be declare in the file with a '.model' statement, the standard way of this declaration is ".model pch TFTSJTU". With those two declaration, this model can be used in the net list. The way to call this model is same with using a sub circuit.

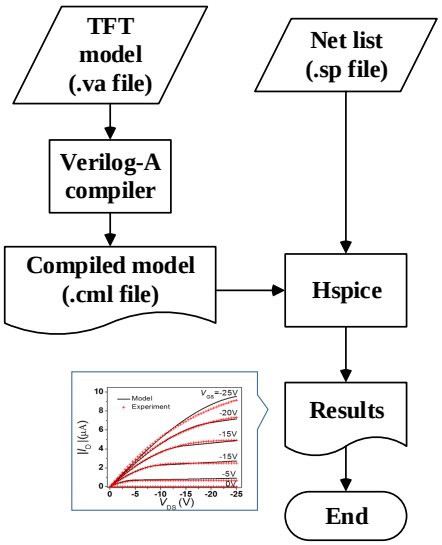

Fig 9 Model implementation in HSPICE

Fig.9 shows the model implementation in HSPICE. After declaring this model in the '.sp' file with '.hdl' statement, HSPICE will try to find the compiled model file (.cml file) under the same path of '.sp' file. If this .cml file is not found, HSPICE will use its Verilog-A compiler to compile '.va' file and generate a corresponding '.cml' file. Embedding this file into the simulation flow, then HSPICE will be able run the simulation. When the simulation is done, the result will be able to be observed in Cscope.

3.1 Model Parameters and Equations

Table 1 states all the parameters that appear in the universal TFT model, their description and value range is also enclosed.

Table 1 Model Parameters

Parameters Name	Description	Range
Version	Version of the model	/
Type	P-type:-1, N-type:1	{-1,1}
W	Channel width	(0:inf)
L	Channel length	(0:inf)
V_t	Threshold voltage	(-inf:inf)
V_{on}	Turn-on voltage	(-inf:inf)

Table 1

Parameters Name	Description	Range
I_0	Off current	(-inf:inf)
*V*ds0	*V*ds applied when I_0 is measured	(-inf:inf)
R_c	Contact resistance	[0:inf)
Lambda	Channel length modulation	[0:inf)
Tox	Oxide thickness	[0:inf)
EPSI	relative dielectric constant	[0:inf)
u0	Mobility	[0:inf)
SS	Subthreshold Swing	[0:inf)
*C*gd	Gate-drain Capacitor	[0:inf)
*C*gs	Gate-source Capacitor	[0:inf)
Off_{21}	Off region up/down warp slope factor 1	(-inf:inf)
Off_{23}	Off region current and V_{DS} relationship	(-inf:inf)
Off_{11}	Off region up/down warp slope factor 2	(-inf:inf)
Off_{22}	Off region up/down warp slope factor 3	(-inf:inf)
$Off_{up/down}$	Off region up warp:1 down warp:-1	{-1,1}

r	Mobility enhancement parameter	[0:inf)

Table 2 describes the equation in different region of the voltage controlled current source used in the equivalent circuit.

Table 2 Equations of the voltage controlled current source

Region	Equation
Saturation (V_{GS}> V_t, V_{DS}>V_{GS}- V_t)	$I_{DS} = K' \frac{W}{L} V_{GSTt}^{\ 2} e^{2v} = K' \frac{W}{L} (V_{GS} - V_t)^{2+\gamma} (1+\lambda V_{DS})$
Linear (V_{GS}> V_t, V_{DS}≤V_{GS}- V_t)	$I_{DL} = K' \frac{W}{L} V_{GSTt}^{\ 2} e^{2v_l} = K' \frac{W}{L} V_{DS} (V_{GS} - V_t)^{\gamma} (V_{GS} - V_t - \frac{V_{DS}}{2})(1+\lambda V_{DS})$
Subthreshold (V_{ON}≤V_{GS}≤V_t)	$I_{SUB} = K' \frac{W}{L} V_{GSTt}^{\ 2} e^{2v} = K' \frac{W}{L} V_{GSTt}^{\ 2} e^{\frac{q(V_{GS}-V_T)\sqrt{1+\lambda V_{DS}}}{nkT(1+\frac{C_d}{C_{OX}})}}$
OFF region 1 (V_{ON}≤V_{GS}≤V_t)	$I_{OFF1} = type \cdot (I_0 \cdot \frac{V_{DS}}{V_{DS0}}^{off_{23}}) \cdot 10^{off_{10} \cdot (type \cdot (V_{GS} - V_{on}))^{off_{11}}}$
OFF region 2 (V_{GS}≤V_{ON})	$I_{OFF2} = type \cdot (I_0 \cdot \frac{V_{DS}}{V_{DS0}}^{off_{23}}) \cdot 10^{off_{21} \cdot (-type) \cdot off_{UP/DOWN} \cdot (-type \cdot (V_{GS} - V_{on}))^{off_{22}}}$

Chapter Four Parameter Extraction

In the compact modeling process of TFT, not only the model should be based on physics but also the associate parameters should have clear physical meaning. Moreover, the extraction method of parameters should also be as simple and straightforward as possible. Once the structure of the model is mature and relatively fixed, a well-established parameters extraction method can then be realize by computer program, which can greatly reduce the workloads of designers. For this purpose, we set up a parameter extraction flow for the proposed universal model, which is shown in Fig.10.

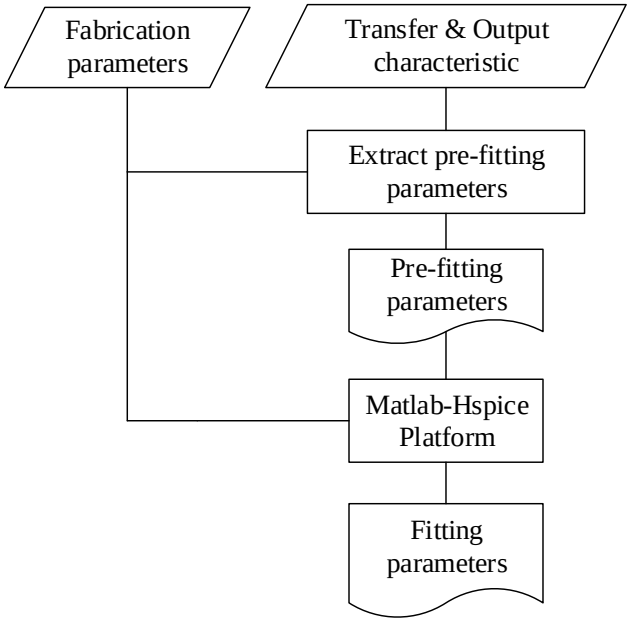

Fig 10 TFT parameters extraction processes

First of all, some fabrication related parameters will be collected. Meanwhile, some parameters like threshold voltage are required to be extract from the output and transfer characteristic of the transistor, those parameters are refered as pre-fitting parameters. It should be clear that all those extracted and collected parameters are not accurate, some of them may need to be slightly changed in next step. Finally, all those parameters will be collected and put into a MATLAB-HSPICE platform, by adjusting

fitting parameters the curve can be fit.

4.1 Extraction of Pre-fitting Parameters

As mentioned before, some of the parameters should have an estimated value before we fit the curve with MATLAB-HSPICE Platform. Those parameters include: contact resistance, threshold voltage and I_O. Here, their typical extraction methods are provided for references.

4.1.1 Contact resistance

The presence of a contact resistance in TFT can be attributed to the metal-semiconductor interface owing to misalignment of metal Fermi level with semiconductor energy levels of interface, as well as the irregular deposition caused poor morphology of organic semiconductor thin film near source and drain metal contacts [15]. The contact resistances share the potential with conducting channel of TFT. The bigger current the TFT generated, the larger voltage drop will be generated on the contact resistance. Without a contact resistance in the model, TFT may provide more current than it should be at high voltage levels.

It has already been proved that contact resistance is different in top contact structure and bottom contact structure [16]. Gate voltage dependent contact resistance models have been proposed too. In this paper, we only consider the condition of bottom contact structures, so the constant resistance is just simply taken as a constant. To extract the value of contact resistance, a transmission line method (TLM) is used. In the linear region, the channel can be taken as a resistor controlled by the gate voltage. Hence the resistance value of the channel reads $R_{CH} \approx L/W\mu C_{OX}(V_G\text{-}V_T)$. Due to the contact resistance located between source/drain electrode and the channel, the total resistance is $R_{Total} = R_C+R_{CH}$. The contact resistance is usually normalized by the channel width W so that it can be universal for devices with different W. Therefore, equation 24 is obtained:

$$R_{Total} \cdot W = \frac{\partial V_{DS}}{\partial I_{DS}} \cdot W = 2R_C \cdot W + \frac{L}{K'(V_{GS} - V_t)} \qquad (24)$$

Based on this equation, devices with different width length ratio should be fabricated at each batch. From these data, we can plot the figure of $R_{Total}\cdot W$ versus L, at a constant gate voltage, the set of $R_{Total}\cdot W$ values exhibits a linear variation. It intercept to the y-axis, and this intercept point is $R_C\cdot W$. If the contact resistor is a constant, then the intercept point will fix at a point which is shown in Fig.11. If the contact resistance vary with gate voltage, the intercept point will change with gate voltage. It should be noted that the uniformity of the devices may directly influence the extraction result of contact resistance.

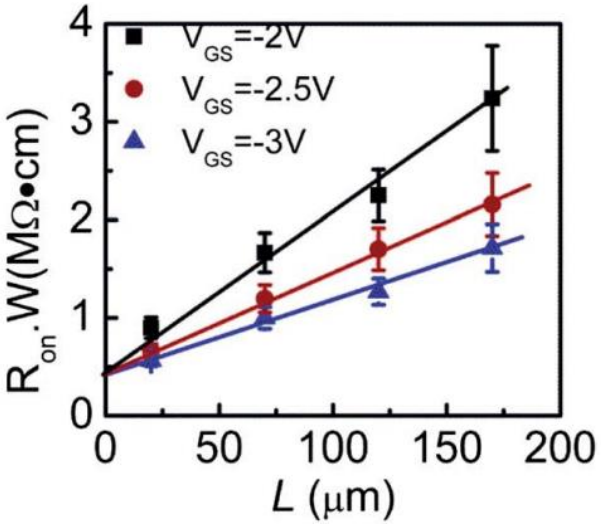

Fig 11 Extraction of contact resistance [17]

4.1.1 Threshold Voltage

Threshold voltage of TFT is the value of gate-source voltage when the conducting channel just begin to connect source and drain electrode. In MOSFET, the threshold voltage refers to the gate voltage when the density of electrons equals to the majority carrier density of the substrate. However, instead of depletion, TFT works under accumulation status. Therefore, the definition for threshold voltage in MOSFET cannot be applied to TFT. The parameter we extract of TFT is an equivalent threshold voltage that used in the current equation.

To extract the threshold voltage, a group of output data will be needed. Assume that the device works as the behavior which MOSFET level 1 describes. As shown in

Fig.12, we need to find the maximum of slope of $\frac{\partial\sqrt{I_d}}{\partial V_G}$ and make a fitting curve (line), then this line will intercept on the x-axis, the value of this point will be the threshold voltage.

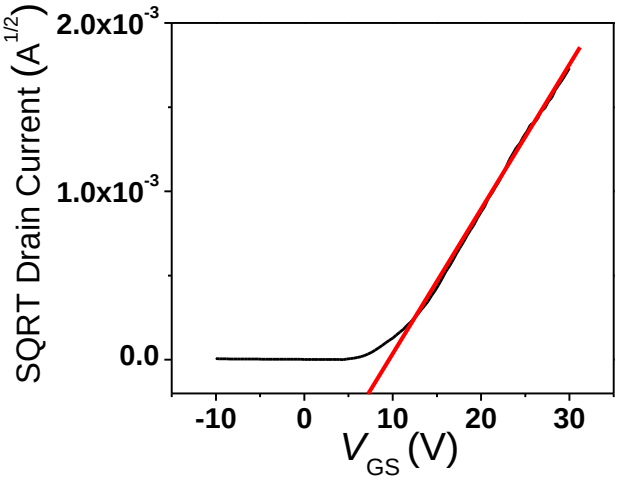

Fig 12 Extraction of threshold voltage

4.1.1 Turn-on Current

In our model, the turn-on current and turn-on voltage have been given a different meaning. Turn-on voltage is the voltage TFT start to turn on, which is about 1V in Fig.13. The turn-on current is the current at turn-on voltage.

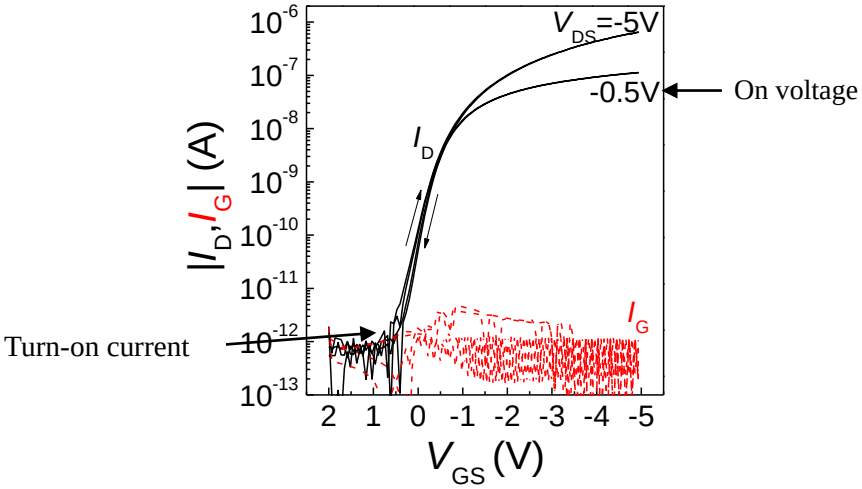

Fig 13 Extraction of on current and on voltage

The extraction of turn-on current and drain-source voltage at turn-on current is

very simple. We can get the value of those parameters directly, turn-on current is the stable current level when device is in OFF region, which can be read from the figure. Since the drain-source voltage is set when the experimental data is measured, drain-source voltage at turn-on current can be obtained directly.

4.1 MATLAB-HSPICE Platform

4.1.1 Platform Structure

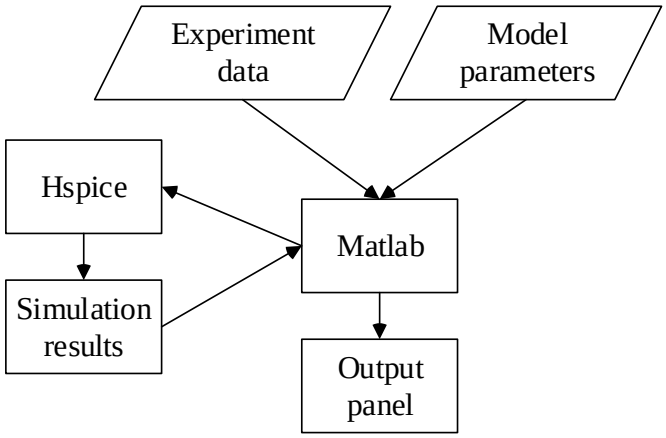

Fig 14 Illustration of MATLAB-HSPICE platform

To reduce the workloads of parameters extraction, a MATLAB-HSPICE platform has been built. For the first time, MATLAB, HSPICE and Verilog-AMS could be run and tested at one time. The function of this platform include: showing the experimental data on the display panel, showing simulation result of the model on the display panel and changing the parameters of model on the input panel. The structure of this platform is shown in Fig.14, MATLAB read the measured data of TFT which is placed in the appointed path and named after transfer.xlxs and ouput.xlxs, respectively. Then a HSPICE input file ('.sp' file) will be generated automatically by MATLAB, this file will be put into HSPICE for simulation, the results of simulation is read and analyzed by MATLAB. Both the measured data and the simulation result will be displayed on a display panel.

4.1.1 GUI of the Platform

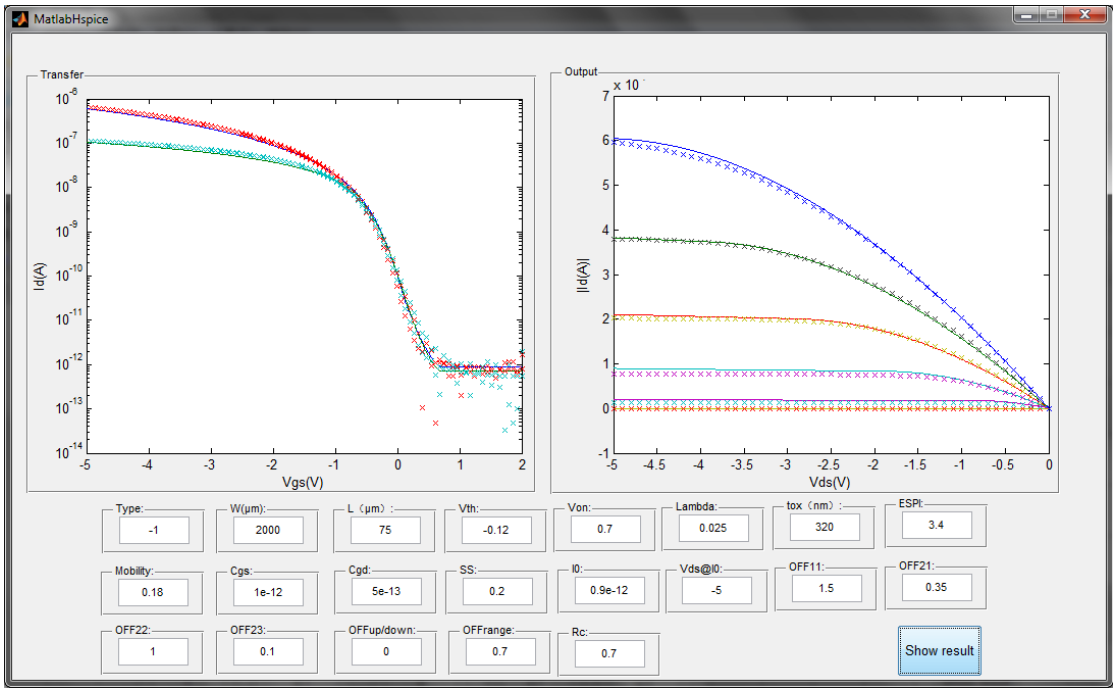

Fig 15 Graphical User Interface of the MATLAB-HSPICE test platform

The graphical user interface of this platform is shown in Fig.15. The front panel of this platform mainly compose two parts: the display panel and parameters input panel. The display panel shows both the original data of experiment and the results of HSPICE simulation, the original data is marked with ‘x’ symbol and the simulation is draw in line. Those two panel shows transfer characteristic and output characteristic, respectively. The input panel shows and provide an easy access to change all the parameters in the model. After writing the parameters into the blanks of input panel, all the parameters in the simulation will be renewed. Then, click the “Show Result” button, MATLAB will call HSPICE simulator to run the simulation. Both experimental data and model data will be showed on the display panel when the simulation is finished.

4.1 Order of Extraction

Notice that all the parameters we have already extracted in the basic parameters extraction stage may not be accurate, especially the thickness and relative dielectric constant of the gate insulator. A compromise to the error brought by the experiment is required to be made. Since the influence of C_{OX} and W/L inaccuracy can be

compensated by adjusting mobility, mobility is changed to fit the curve so that both C_{OX} and W/L remains the expected value regardless of the difference between real value and the input value.

When every parameters are set, the curve of simulation result may still unable to be close to the experimental data. This is might due to the process variation between device and device. Some of the input parameters will needed to be adjusted slightly so that a smaller relative error can be achieved. However, parameters should not be changed to a value that disobey the physical rules.

Based on the principles mentioned above, the curve can be fit based on the order of parameters extraction stated in the following paragraph:

1) Extract threshold voltage parameter V_t (Change V_t until the subthreshold region is in the suitable position of the transfer characteristic)
2) Extract mobility parameters μ_0, γ. (Change μ_0 until the current in the saturation region of output characteristic is at the same level of the measured data, at the same time, γ should be changed to ensure the linear region has the appropriate slope)
3) Extract the channel length modulation parameter λ to fit the curve. (Change λ until the latter part of saturation current is fitted)
4) Slightly adjust the contact resistance R_C to fit the high voltage level current. (Change R_C until all levels of current is fit)
5) Adjust turn-on parameters I_{ON}, V_{ON}, which is used to set the range of subthreshold region. (Adjust V_{ON} to set the voltage range, adjust I_{ON} to set the current range)
6) Extract the subthreshold swing parameter SS. (Change SS until the slope of subthreshold region is completely fit)
7) Extract off region parameters. (Change $Off_{up/down}$ to selected the OFF region current mode, then adjust Off_{21} and Off_{22} to change the slope of OFF region current, finally adjust Off_{23} to change the relationship between OFF region current and V_{DS})

Chapter Five Verification of the Model

In this chapter, a series of modeling tests are run to verify the accuracy and universality of the proposed model. Those test benches covers different materials and different processes, including two different small molecule OTFTs, a polymer OTFT and an IGZO TFT. Tests results show that this model is accurate and can reflect major behaviors of different TFTs.

5.1 Small Molecule OTFT

In this test, a bottom-gate bottom-contact small molecule OTFT is selected as the first fitting object. The device structure and the materials that has been used are illustrated in Fig.16. In the device fabrication process, 40nm aluminum metal layer was thermally evaporated onto the substrate (glass) as the gate electrode at the beginning. Then polyvinyl-alcohol (PVA) was spin-coated and cross-linked on the sample. A 40nm source and drain electrode was evaporated onto the sample through a shadow mask. Finally, the semiconductor layer (TIPS-PS blend) is spin-coated on the sample.

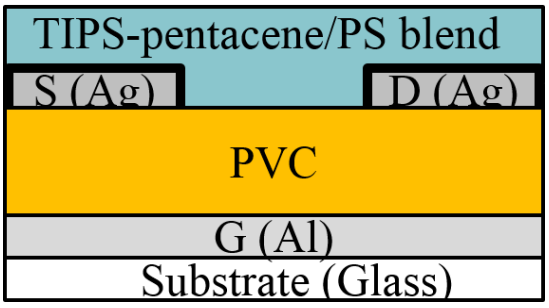

Fig 16 Schematic diagram of the first small molecule OTFT sample

Small molecule OTFTs usually have relative small subthreshold swing and can operate at low voltage, this differentiate it from other TFT technics. Those features should be reflected in the model for this device.

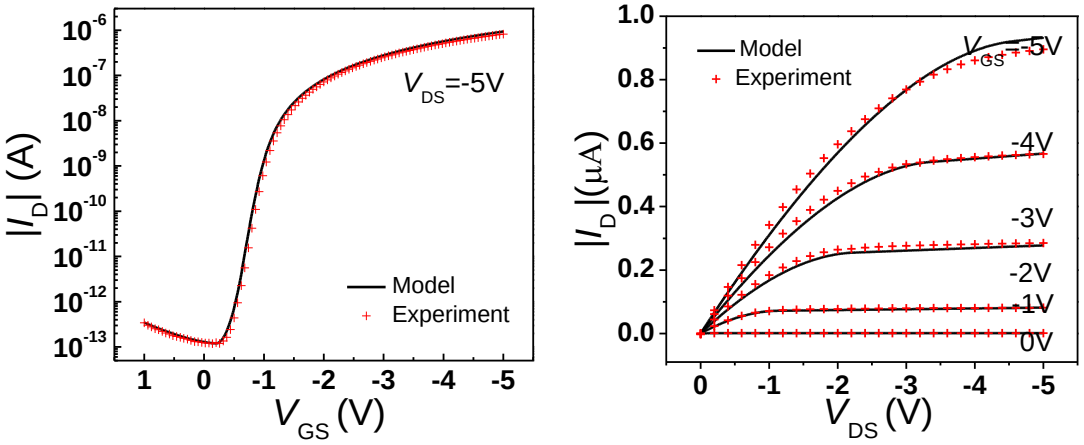

Fig 17 Test results of the first small-molecule OTFT sample

Fig.17 shows the test results of the first sample small-molecule OTFT, an excellent agreement can be observed. Its parameters are summarized in table 3. This result proved that this universal TFT model can reproduce the behavior of this small molecule OTFT sample.

Table 3 Parameters of the first small molecule OTFT model sample

Parameters Name	Value	Parameters Name	Value
Version	2.2	Lambda	0.04 1/V
Type	-1	tox	255nm
W	1200μm	EPSI	3.4
L	70μm	Mobility	0.9cm^2/V s
V_t	-0.9V	C_{gd}	1pF
V_{on}	-0.2V	C_{gs}	1pF
I_0	1.2e-13A	V_{ds0}	-5V
R_c	0.5e6Ω	Off_{11}	2
Off_{21}	0.35	Off_{22}	1.5
Off_{23}	1	$Off_{up/down}$	1

To show the tolerance of this model to the variation of processes, an all solution-processed small molecule OTFT is chose as the second sample. The device structure and the materials that has been used are shown in Fig.18. At the beginning of the device fabrication process, a polyvinyl chloride polymer (PVC) buffer is spin-coated onto the polyethylene naphthalate (PET) subtrate. Then the gate electrode is printed by an inkjet printer with sliver ink. After that, another layer of PVC was spin-coated and cross-linked on the sample, this layer is used as dielectric. Next, source and drain electrode was printed onto the sample. Finally the semiconductor

layer (TIPS-pentacene-PS blend) is spin-coated at the top of the sample.

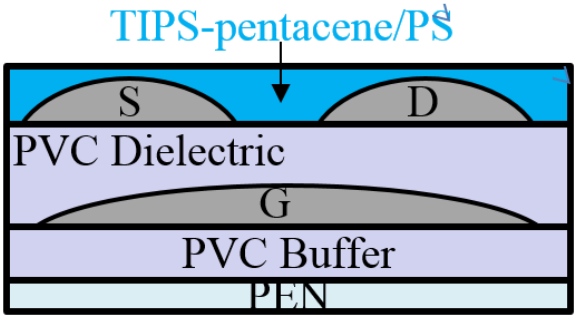

Fig 18 Schematic diagram of the second small molecule OTFT sample

Compared with partial solution-processed OTFT, this all solution-processed OTFT model have a bigger subthreshold swing because the C_{OX} of this device is smaller, but it have a smaller contact resistance since its printed electrodes has a smaller misalignment of metal Fermi level with semiconductor energy levels. Those features should be reflected in the final result of the model.

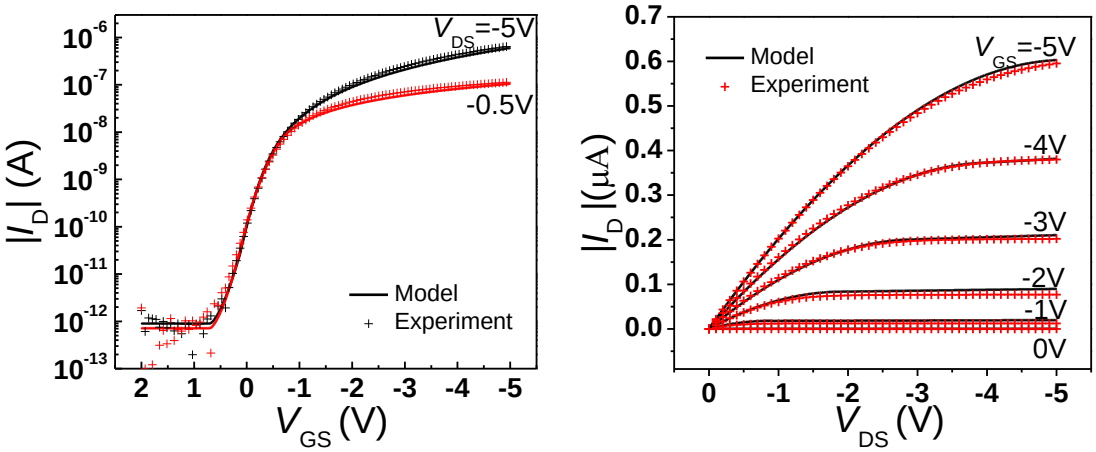

Fig 19 Test results of the second small molecule OTFT sample

The test results of the all solution-processed small molecule OTFT is shown in Fig.19, the proposed model can match this all solution-processed devices perfectly. The used parameters in the model is shown in table 4.

Table 4 Parameters of second small molecule OTFT model sample

Parameters Name	Value	Parameters Name	Value

Version	2.3	Lambda	0.025 1/V
Type	-1	tox	320nm
W	2000μm	EPSI	3.4
L	75μm	Mobility	0.18 $cm^2/V \cdot s$
V_t	-0.12V	C_{gd}	5pF
V_{on}	0.7V	C_{gs}	1pF
I_0	1.2e-13A	V_{ds0}	-5V
SS	0.2V/decade	Off_{11}	1.5
R_c	1e6Ω	Off_{22}	1
Off_{21}	0.35	$Off_{up/down}$	0
Off_{23}	0.1	Off_{Range}	0.7

5.1 Polymer OTFT

In this section, a polymer OTFT is selected to be the third test bench. Its structure and the materials that has been used are shown in Fig.20. In the device fabrication process, the source and drain electrodes are thermally evaporate on the substrate (Glass) first. Then the polymer semiconductor materials provided by imperial college are spin-coated on the sample to fabricate the conducting channel. Then a layer of Cytop is spin-coated to form the dielectric. Finally the gate electrode is evaporated on the top of the sample.

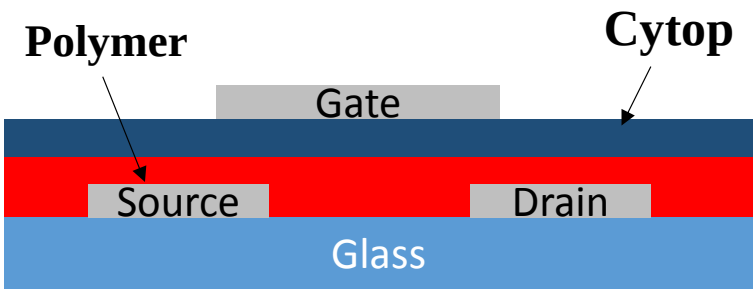

Fig 20 Schematic diagram of the bottom-gate bottom-contact structure polymer OTFT

Compared with the small molecule OTFT, polymer OTFT have a much bigger subthreshold swing, its working voltage is also much higher than the small molecule OTFT.

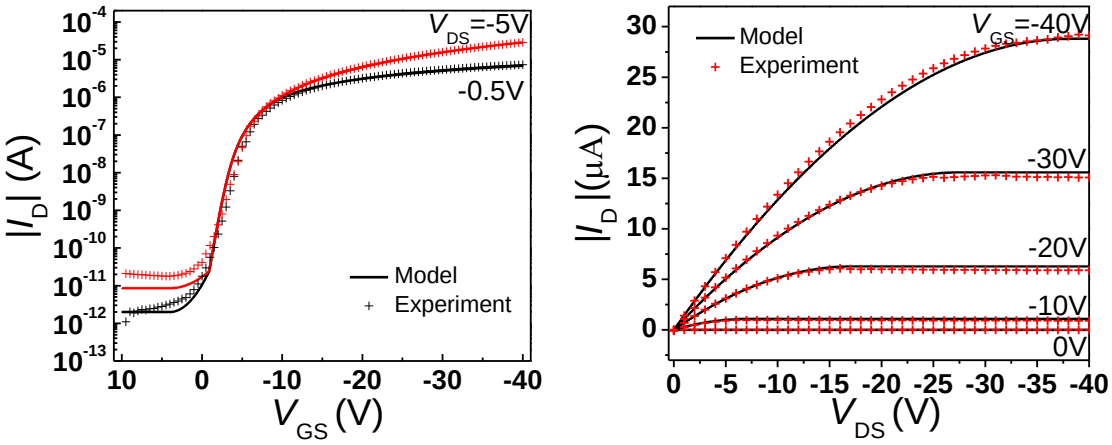

Fig 21 Test results of the small-molecule OTFT (with evaporation processes)

The test results of all polymer OTFT is shown in Fig.21, the proposed model can match this high operating voltage devices very well. The used parameters in the model is shown in table 5.

Table 5 Parameters of small molecule OTFT model (all solution-processed)

Parameters Name	Value	Parameters Name	Value
Version	2.3	Lambda	0.001 1/V
Type	-1	tox	800nm
W	1000μm	EPSI	2.1
L	75μm	Mobility	1.35 $cm^2/V \cdot s$
V_t	-0.3V	C_{gd}	1pF
V_{on}	4V	C_{gs}	1pF
I_0	2e-12A	V_{ds0}	-5V
SS	0.8 V/decade	Off_{11}	2
R_c	4e5Ω	Off_{22}	1
Off_{21}	0.35	$Off_{up/down}$	0
Off_{23}	0.7	Off_{Range}	0.7

5.1 IGZO TFT

In this test, we collaborate with Dr. Di Geng and Mr. Yuanfeng Chen in Kyung Hee University, Korea. With their mature processes for IGZO TFT, we are able to test the compatibility with IGZO materials.

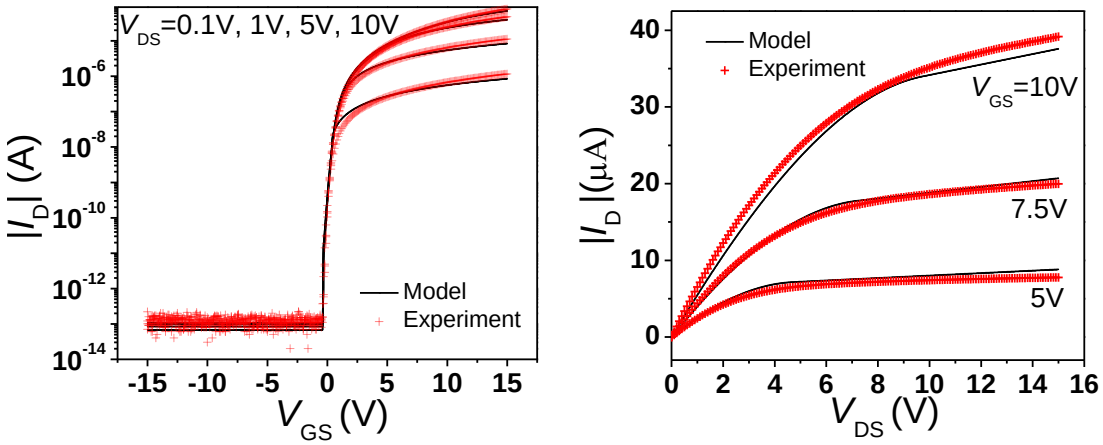

Fig 22 Test results of the IGZO TFT

Fig.22 shows the test result of IGZO TFT. The proposed model can match this inorganic devices very well. The used parameters in the model is shown in table below.

Table 6 Parameters of small molecule OTFT model (all solution-processed)

Parameters Name	Value	Parameters Name	Value
Version	2.3	Lambda	0.025 1/V
Type	1	tox	800nm
W	20μm	EPSI	2.1
L	6μm	Mobility	75 $cm^2/V \cdot s$
V_t	0.3V	C_{gd}	1pF
V_{on}	-0.4V	C_{gs}	1pF
I_0	1 e-13A	V_{ds0}	5
SS	0.2 V/decade	Off_{11}	3
Off_{21}	0.35	Off_{22}	1
Off_{23}	0.1	Off_{Range}	0.2

5.1 Summary

In this chapter, we test the model with four different kinds of TFTs, those tests covers three kinds of materials and three different structures. This model can fit the characteristic of BGBC, BGTC and TGBC devices accurately. The impacts of different materials on the device performance can also be reflected very well in this model.

Chapter Six Circuits Simulation Tests

Now that this model has proved its compatibility with different kinds of TFTs, further test conducted on circuit simulator (HSPICE) can then be carried out. In this chapter, DC and transient tests are carried out to test this model. Experiment data of those tests are collected from Advanced Display Research Center at Kyung Hee University. The IGZO TFT model used in the simulation is the same one mentioned in section 5.4, this TFT is fabricated in the same batch with the inverter. DC simulation result matches the original data, however, transient simulation have a larger error, those results have been carefully investigated and an explanation for the phenomena are provided too.

6.1 DC Test

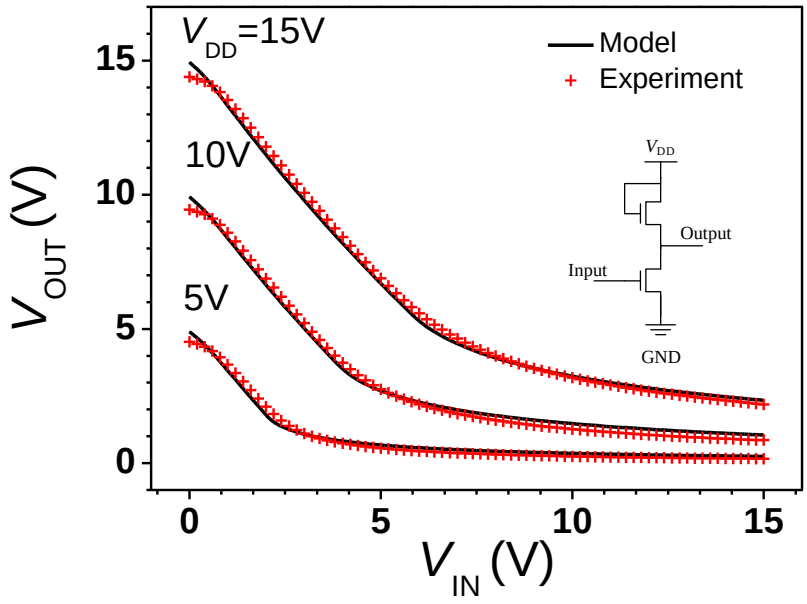

Fig 23 Static measurement of the diode-load IGZO TFT inverter

In this section, a DC test is carried out to test this model. A diode-load inverter is

selected as the sample. As shown in Fig.23, this inverter is consisted of two IGZO TFTs. The upper one in the figure is the load TFT, whose gate and drain are connected together. The source of load TFT is connected to the output node of the inverter. The lower one is the driving TFT, its gate is used as the input of the inverter, its source is connected to ground and its drain is connected to the output node. The *W/L* ratio of those two TFTs are cautiously selected to achieve the maximum noise margin. The W/L ratio of the load TFT is 100μm/6μm, and the W/L ratio of driving TFT is 300μm/6μm. The inverter is test with three different supply voltage which are 15V, 10V and 5V, respectively.

As long as the inverter is powered with supply voltage, the load TFT will work in saturation region because $V_{DS}=V_{GS}>V_{GS}-V_T$. In contrast, the driving load need to work in OFF region, linear region and saturation region successively with the increase in input voltage. When the driving TFT works in saturation region and linear region, the simulation results match very well with the measured transfer characteristic. But when driving TFT works in OFF region, a little difference can be observed between simulation result and measured data. This error is acceptable because the data we used in OFF region modeling have an error which is caused by measurement equipment.

Therefore, this test proves that this model have a good DC accuracy in all the working region.

6.1 Transient Test

As one of the most important function in circuit simulator, transient test should be carried to verify this model. In the transient test, not only the accuracy of current function and the rationality of equivalent circuit is tested, but also the capacitor model is verified.

Transient response of the diode-load inverter to a square ware is measured when the inverter is biased with a supply voltage of 15V, peak-peak value of the input square wave is 15V and its frequency is 50 kHz.

Simulation result of this inverter is shown in Fig.24, the data of simulation results have a very obvious glitch when the inverter output a high voltage signal, this

occurrences happen when the driving TFT works in the OFF region and the load TFT works in the saturation region. Technically speaking, this glitch won't happen as long as the output characteristic of driving TFT can intercept with the characteristic of the diode load I-V curve. After looking into the simulation report of this circuit, we believe that this glitch is cause by the non-convergence of the simulator. Due to the defects in the first order derivative continuity between OFF region and saturation region, the circuit simulator automatically choose a mode whose primary target is to conclude the project, but this mode will reduce the accuracy of simulation. As a result, this glitch occurs in the simulation. To eliminate this glitch, the smoothing function between OFF region and saturation will need to be modified. In a strictly test, not only the first order derivative should be continuous, but also this second derivative of the model current equation should be continuous. Therefore, the glitch is caused by the error of the simulator, this can be avoided by modified the smoothing function between OFF region and saturation region.

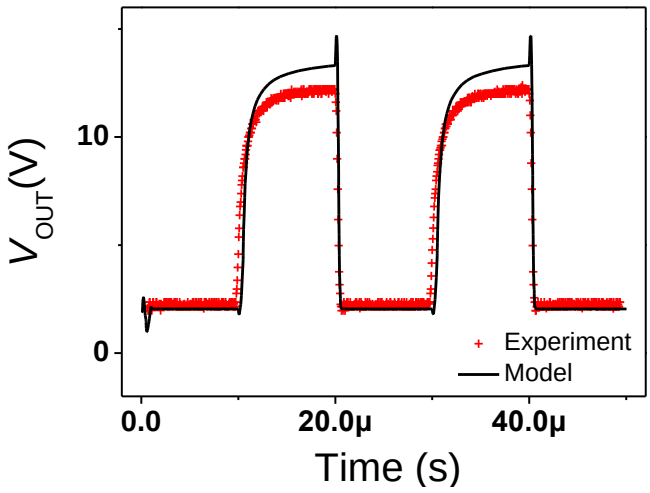

Fig 24 Transient measurement of the diode-load inverter

The simulation results fit the experimental results well as shown in Fig.25, proving the feasibility of using this model in commercial circuit simulators for simulation and predicting TFT circuit performance.

Chapter Seven Summary and Future Work

7.1 Summary

In this dissertation, a universal TFT model is designed. Though there is still a long way to go for this model to be widely accepted in academic circle or be used in mass production in industry, an important attempt has been made to build a TFT model that can be compatible with different kinds of TFTs. The significance and innovation of this dissertation can be summarized into the following paragraph:

1) A new concept of compact modeling has been proposed in this dissertation. In comparison with the traditional models, this newly-proposed model is designed on a cutting-edge purpose, which is building a universal model for newly-developed devices. This model has the ability to describe the essence of TFT behavior, at the same time, some parameters are merged to simplify the current equation. Therefore, even if we do not fully understand the working mechanism of the newly-developed devices, we can still apply this model on it. As a result, newly-developed devices can transition from scientific experiments to practical devices at a much faster pace.
2) Decrease in the number of parameters also makes parameter extraction easier. In this dissertation, a parameter extraction platform is set up with MATLAB and HSPICE. Although users still need to do a lot of operations during the extraction, the order of parameter extraction stated in this dissertation enables us to extract the parameters efficiently, besides that, this order can become an important guidance to design an auto parameter extraction software.
3) Based on the application of this model stated in Chapter 7, it can easily occur to us that this model can be used to design a complex system. As one the most fundamental components in digital circuit, the successful simulation on an inverter enables us to conduct more complex simulation based on this model. We believe that this model can be used in analog design as soon as an

accurate capacitor is added into the model.

From those facts mentioned above, I believe this research is highly valuable and may create commercial value in the near future.

7.1 Future work

A universal TFT model is established in the dissertation, but this model is not sufficiently mature to be used in manufacturing. Therefore, to realize the goal, more work should be carried out to reform and improve this model based on this dissertation. Some of the work that need to be carried out in the future is listed in the following paragraph:

1) This model is based on the assumption that the semiconductor's density of states is exponentially distributed. However, the actual density of states may have many forms. Therefore, a mobility model that support different kinds of density of states should be designed and implement into the model.
2) A good capacitor model is very essential to build an accurate TFT model, in this dissertation, the capacitor model is cannot precisely reflect the behavior of TFT in transient simulation. Hence, an accurate but simple capacitor model is expected to be built in the future.
3) An auto parameter extraction software should be built based on the principles mentioned in section 4.3. This software will greatly reduce the work load of user.

I believe this model will be constantly improved, and it will be widely accepted. I hope this model can push forward the development of TFT, and it can have a positive influence on our life in the near future.

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